IN THE ABSTRACT:

Please Amend the Abstract as follows:

A frequency divider ~~comprising~~ includes a first flip-flop (M1, M2, M3, M4) having a first clock input (CI) for receiving a clock signal, and first ~~the~~ flip-flop ~~further comprising~~also includes a first set input (Q4) and a first non-inverted output (Q1). ~~The frequency divider further comprises a~~ A second flip-flop (M', M', M', M') ~~having~~has a second clock input (CI) for receiving a second clock signal that is substantially in anti-phase with the clock signal inputted into the first clock input (CI), and a second set input is coupled to the first non-inverted output (Q1)~~.~~, ~~a~~A second non-inverted output (Q2) and a second inverted output (Q2) are arranged so that ~~,~~ the second inverted output (Q2) ~~being~~is coupled to the first set input (Q4).